Application Bulletin AB-14

Isolating Data Converters—What's All The Noise About?

Why Isolate Data Converters?

As we'll show in this bulletin, isolation is a cost-effective way to reduce data converter system noise and increase resolution. The bulletin shows how "best in class" distortion specs can be achieved with the correct mix of isolation and appropriate ground plane PCB layers.

Data Converters

Data conversion products such as Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) are among the most complex mixed signal devices ever designed. In the digital age, they are at the heart of all real world interfaces and are used to control every imaginable system. Optimizing noise performance is perhaps one of the most difficult challenges in converter applications because of the insidious nature of the noise signal. Noise is always difficult to measure and even more difficult to calibrate. Just the act of measuring noise in a system can change analog and digital signal paths and produce false readings.

At the chip level, data converter design engineers go to tremendous lengths to separate analog and digital ground currents. It is impossible to overstate the fact that electronic layout of the converter device is the limiting factor in noise performance in any generation of converters, and separation of currents, both ac and dc, desired and parasitic, is the most challenging aspect of any design. It's important to remember that the best possible performance these devices will ever deliver is on the manufacturer's test system. Millions of dollars are spent to ensure the parameters of the device are accurately measured and specifications are pushed to the absolute limit within the constraints of the semiconductor process employed. Unlike in practical applications, the chip manufacturer doesn't need to worry about the nuisance of other devices on a PCB, multiple power supplies, the constraints of cost and a host of other noise headroom detractors, meaning it's always more difficult for you, the designer, to get even close to the theoretical device performance. This application note walks through the traditional methods of maximizing performance in converter applications and shows how IsoLoop® Isolators can be used for optimal separation of analog and digital ground currents, boosting system noise performance.

Splitting Current Paths

If you've just tested your new data acquisition design and were disappointed that the 92 dB signal-to-noise+distortion ratio you expected is closer to 80 dB, you're not alone. Realizing the true potential of a high-accuracy ADC is a mix of picking the right converter for the application, applying the most effective signal conditioning in the ADC input "physical layer," and separating the digital and analog signal paths as best you can. Mistakes can be made in all three of these steps, but by far the most common source of converter error is in the treatment of analog and digital signal paths.

Figure 1 shows a typical ADC application as drawn by the designer:

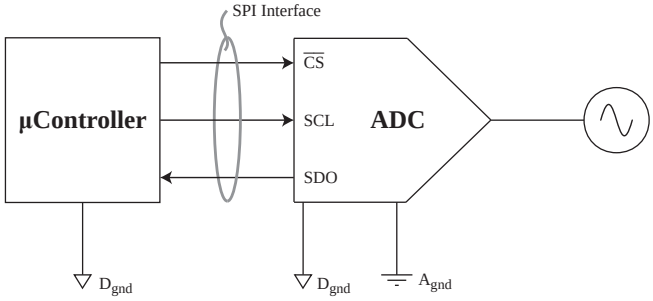

Fig. 1. Typical ADC Circuit

Separate analog and digital grounds are shown. On the board, these grounds must be connected together then routed to system ground. Figure 2 shows the same circuit, but with analog components representing the layout traces:

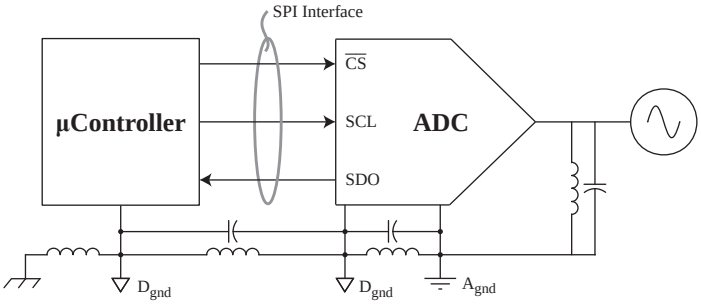

Fig. 2. ADC Circuit Illustrating Parasitic Components

Capacitance and inductance couples the grounds to each other and the input signal. Care needs to be taken here. Converter manufacturers normally recommend connecting the analog and digital grounds as close as possible to the chip. That's sound advice, but lacks detail. In the case of an ADC, consider what happens during normal operation: an analog signal is sampled and the digital representation of the voltage is output as a digital word. Most ADCs have CMOS output stages to reduce power consumption. Since CMOS draws power during state changes, there is a considerable variation in instantaneous digital ground current as the input voltage, and therefore the converted output code, changes. This change in ground current will change the effective input voltage seen by the ADC if there's enough impedance back to system ground. In other words, it's important to not only connect the grounds together, but to make sure the impedance of the resultant ADC ground to system ground connection is as low as possible. The usual solution is a ground plane connecting analog and digital grounds right under the device. This certainly appears to be the best option, but beware of the pitfalls. Busy circuit boards with multiple layers may have several foil layers dedicated to ground current return. At the very least, a dense PCB could have signal tracks crossing over ground planes. If you're designing with a high speed ADCs or DACs, it's important to remember that track crossings could have a detrimental effect on the very specs you spent a fortune on the converter to realize. Any circuit trace crossing any other with an insulating board layer between them forms a parasitic capacitor. If your board has multiple crossing tracks on the digital I/O, or there are parallel ground planes, CMOS switching transients will induce instantaneous error currents in your analog circuits faster than you can say CdV/dt. The FFT plot in Figure 3 helps illustrate the key dynamic specs:

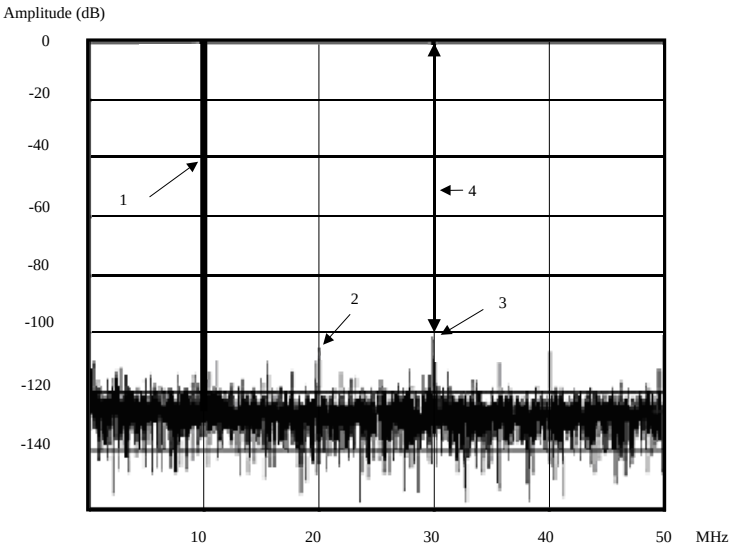

Fig. 3. 16-bit ADC FFT, V(f) 0dB, 10MHz

The fundamental (1) has first and second harmonics at (2) and (3). Spurious Free Dynamic Range (SFDR) is limited by the largest distortion spur and is illustrated by (4). Signal-to-Noise ratio (SNR) is calculated with the familiar Equation 1, which ties SNR to quantization error of a number of bits (n):

$$SNR = (6.02n + 1.72)dB \quad \text{..... Eqn. 1}$$

This yields an SNR of 98 dB in the example above.

The most important specification for almost all sampling systems, however, is Signal-to-Noise Ratio plus Distortion (SINAD) and its resultant application-limiting Effective Number of Bits (ENOB). Unlike SNR, SINAD takes into account all noise from all harmonics. It is the ratio of fundamental signal power to the power of all harmonic noise plus the power of all spectral distortion. ENOB is calculated by replacing SNR in Equation 1 with SINAD and rearranging:

$$ENOB = (SINAD-1.76)/6.02 \text{ bits} \quad \text{... Eqn. 2}$$

Digital noise currents in fast CMOS circuits are a large part of the high frequency noise error spectrum in a typical converter system. ENOB is the limiting specification in telecom, audio, video, photo and many industrial applications, including delta-sigma systems. Careless design can unnecessarily limit this figure of merit.

How Do IsoLoop Isolators Help?

All isolators have an inherent ability to route currents where designers want them because of their very large isolation barrier resistance. If you could place a 300 GΩ resistor between analog and digital portions of your circuit you'd do it, right? Not quite. Optocouplers aren't used for high speed current routing in converter circuits because their parasitic capacitance adds more distortion and noise than the original circuit. Most non-optical isolators have high EMC footprints and are an unwelcome sources of additional noise. IsoLoop isolators change all that and allow the designer to effectively segregate digital and analog ground current paths without additional noise:

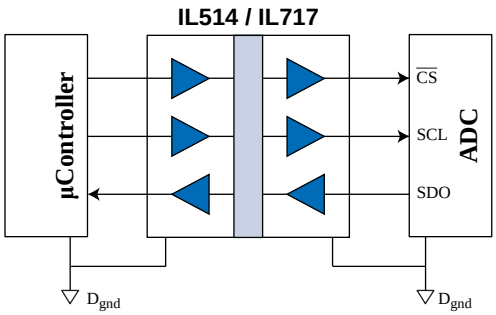

Fig. 4. Isolated ADC Circuit

An IL514 isolator provides three channels of isolation, 25 ns propagation delay, and 10 ns pulse-width distortion. An IL717 provides four channels, 10 ns propagation delay, and just 3 ns pulse-width distortion.

High speed digital isolation allows the converter to function as it did on the manufacturer's test head with the minimum level of digital interference, and is as close as it gets to perfect current steering outside the chip. In high-speed systems, digital slew rates can be as high as 5 kV/µs, with ground bounce in motor control and power conversion applications slewing higher than 10 kV/µs. At a rate of change of 5 kV/µs, it only takes a 200 fF capacitor to inject a 1 mA spike into a sensitive analog input node. Input voltage, or rather output code-dependent charge injection from asynchronous noise sources, is one of the key reasons the SFDR of an ADC in an application is usually less than that specified by the converter manufacturer.

What's the Cost?

If isolation works miracles on noise, does that mean it costs too much for most applications? No. Each additional layer of a multiplayer PCB adds about 20% to the board cost. An IL514 isolator costs about $0.50 per channel, so the trade off between extra layers and active current steering becomes attractive in a hurry. Even without the trade-off in PCB cost, what is it worth to be able to go to your Marketing VP and make the case that a $1.60 component could boost your system ENOB by 0.5 bits, differentiating you in those high resolution optical markets, or that it could add 1% to your total call load per telecom base station. Reducing digital current noise can create a huge advantage in digital data systems because of its promise to let the user push the envelope in accuracy, effective resolution, and bandwidth with the same basic hardware.

PCB Layout

Placement of the ADC is a critical part of the layout. The ADC as close as possible to the side of the board with circuit power and signal input minimizes parasitic ground current paths and improves dynamic performance. Each pad of a surface mount circuit board provides about 100 fF of capacitance to the ground plane or track beneath it. If the layout of Figure 5 is used, high-speed return currents will be injected into the analog signal path:

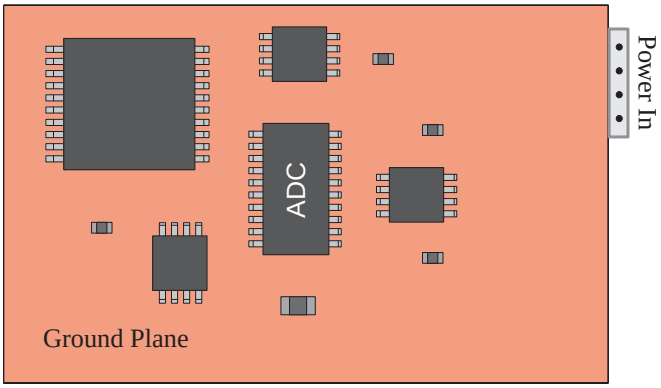

Fig. 5. High Noise ADC Location

Moving the ADC closer to the supply and physically routing all non-ADC currents as shown in Figure 6 can reduce the effect:

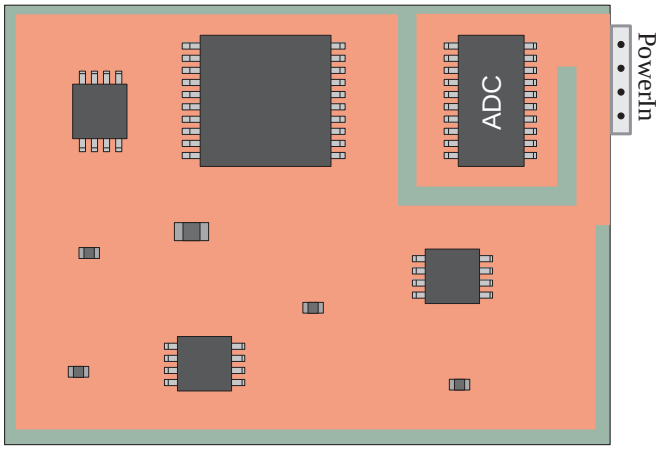

Fig. 6. Improved Grounding

In Figure 6, ground current returns from other parts of the circuit board do not travel across, under, or in parallel with ADC analog signals, reducing the effect of any high-speed transients. Coupling is, however, present in the digital ground and digital I/O lines of the device.

Figure 7 shows the layout of the Figure 4 circuit with an IsoLoop isolator. This substantially reduces asynchronous noise current by inserting a high impedance between the digital ground of the microcontroller and the digital ground return of the ADC:

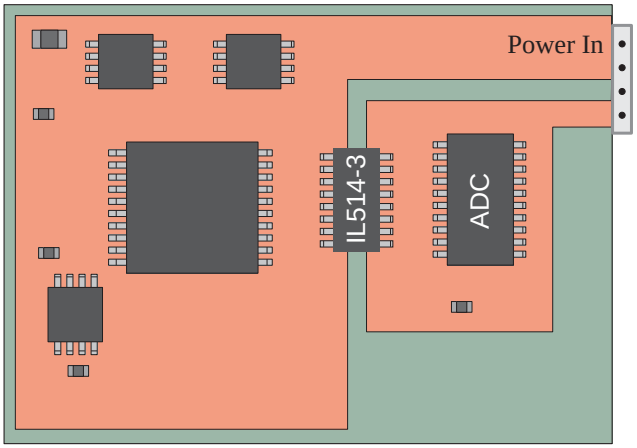

Fig. 7. Isolated ADC Board Layout

The isolated ground of the IsoLoop isolator is connected to the analog reference ground of the circuit board, and this time all digital currents into and out of the ADC are from ADC digital I/O activity and are synchronized to the conversion clock or data clock. Unlike the improved passive layout in Figure 6, there is no asynchronous noise injected into the ADC ground from the rest of the digital circuits on the board.

Figure 8 shows Kirchoff's current loop for Figure 6, while Figure 9 shows the loop for the isolated board in Figure 7:

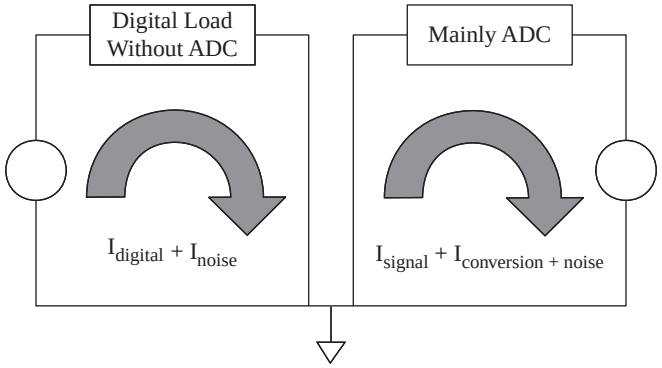

Fig. 8. Kirchoff's Loop for Layout of Figure 6

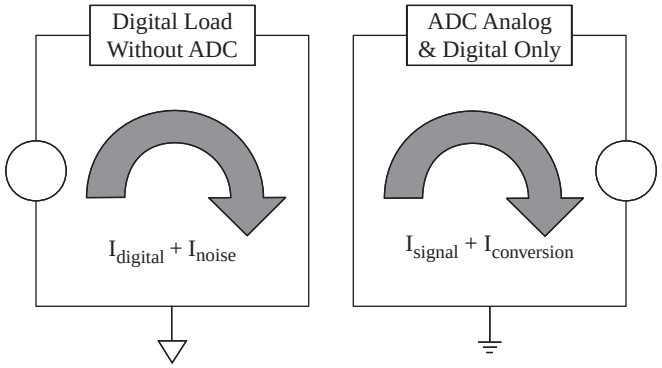

Fig. 9. Kirchoff's Loop for Layout of Figure 7

Note how in Figure 9 the isolator effectively blocks all currents from the ADC loop that are not generated by the ADC. Asynchronous, fast rise-time current spikes are effectively routed to the ground terminal without interfering with the analog signal.

Conclusion:

Digital Signal Isolation and Current Steering

Complete galvanic isolation between an ADC and the rest of the board components is achieved by using a second power supply and returning grounds from both sections of the board to their respective grounds. Steering digital currents in this way is a powerful method of upgrading converter noise performance.

Careful selection and layout of the isolated power supply is required to prevent the superposition of supply noise into the analog signal path of the converter, but an isolated converter circuit provides a great deal of noise performance improvement.